REMARKS

Independent claims 51 and 53, and dependent claim 51 were previously presented. Minor amendments have been made to correct grammar and to conform the claim language as between the various pending claims.

Claims 66 - 73 have been previously withdrawn as they are directed to a separate invention.

The method claim 53 does not fall within the prohibitions of In Re Bilski as there is particular claimed hardware, such as the buffer, which must be used in conjunction with the method steps. Further, as noted in the specification "since the frame arrival rate is extremely fast at gigabit link data rates, the FOPL must act in real time". These systems operated at gigabit speed. They cannot, as suggested in the Office Action, be handled on paper.

All of the claims require that the improved buffer overrun prevention logic accomplish four (4) distinct results, namely that:

(1) the buffer overrun prevention logic **tag, but not terminate**, words that overrun the buffer,

(2) set the tag bits to a **unique value indicative of an overrun condition**,

(3) operate on the tag bits and **not the data bits**, and

(4) store the tag bits in the buffer with data bits, which **tag bits indicate that the overrun word is to be aborted**.

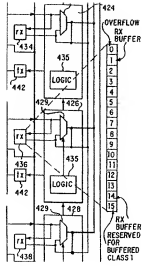
The specification as originally filed contained a very detailed description of the structure and operation of the FIFO Overrun Prevention Logic (FOPL). Figs. 5 and 8 detailed the FOPL, and the text (found at col. 23, lines 41 - 63 in parent USP 6,185,203) provided detailed support for these four items as follows.

> The purpose of the FOPL is to handle the case where the FIFO 155 is full and frames are received by the Endec 153. Since the frame arrival rate is extremely fast at gigabit link data rates, the FOPL must act in real time. An additional situation the FOPL must handle is when the frame arrives and is being routed to the remote port and the back end of the frame overruns the FIFO. Still another situation is where multiple frames overrun the FIFO. **(2) The FOPL operates on the TAG bits 154 not the data bits** 171. The Endec takes gigabit serial transmission from the link side, decodes the transmission and outputs thirty two bit words to the port control FIFO. Along with the thirty two bit words are a two bit tag field and a two bit parity field. The tag and parity field additions are a common interface characteristics. Tag bits are bits attached to the thirty two bit words to indicated delimiters such as the SOF or EOF. When the FIFO is full and a frame is received from the Endec the FOPL sets the tag bits to an illegal value. When the FIFO enters the not full condition the next word will contain the illegal tag bits. The **(3) illegal tag bits** will signal the Port Control module to **(4) abort the frame** with the appropriate EOF delimiter.

The specification uses the term "illegal" tag bits, where that is to be understood to mean something other than the "tag bits are bits attached to the thirty two bit words to indicated delimiters such as the SOF or EOF", i.e., start of frame or end of frame. Applicant uses the new and different tag bits to indicate to Port Control module that it needs to abort the frame. That they are "illegal" merely highlights the manner in which the improvement operates distinctly different from the prior art.

Bennett USP 5,592,160 dedicates a single, fixed length buffer to addressing overflow. Bennett provides at col. 5, lines 58 to 67, with the relevant portion of Fig. 4 being reproduced, below, for the Examiner's convenience:

> Each receive memory 432, 434, **436** and 438 is comprised of a set of sixteen memory buffers numbered 0-15 (illustrated in the expanded portion 440 of FIG. 4), **each having a storage capacity of two kbytes**. Memory buffers numbered 1 through 14 are designated for frame transfers of class 2, memory buffer numbered 15 is reserved for class 1 frames destined for the embedded N.sub.-- port on the element controller 358 (FIG. 3), and **memory buffer number 0 is reserved for overflow**. A maximum size frame in accordance with the Fibre Channel industry standard is 2148 bytes long.



While the Office Action at page 4, line 5 suggest that Bennett include buffer overrun prevention, item 436 is just the overflow buffer. There is no "prevention" of the overflow. There is simply a fixed length, single buffer, and if it overflows, it overflows. Bennett does not in any sense prevent the overflow, and there is but a single structure, the buffer itself, not **2** structures as claimed, namely, a buffer and buffer overrun prevention logic. The rule against double inclusion precludes the use of the same structure (the mere buffer 436) to meet 2 limitations of the claim.

The secondary reference Gulick does not fill the omissions in Bennett, but rather teaches away from applicant's claimed invention. Rather than performing the claim limitation of tagging "but not terminating", Gulick does the exact opposite. The Office Action recognizes this (OA of 2/9/09, page 4, line 14), as it must, Gulick is perfectly clear in this regard. (Gulick, Col. 30, line 35 "…FIFO overrun condition exists. When this happens the packet is terminated…").

Further, while the last byte may be tagged, it is tagged as "the last byte in the packet". (Gulick Col. 30, line 35). It is not tagged as required by the claim to "indicate that the overrun word is to be aborted". Again, Gulick teaches away in that it uses an ordinary tag (end of packet), not applicant's "illegal" tag to cause the frame to be aborted.

The Supreme Court decision of *KSR v. Teleflex*, 127 S. Ct. 1727, 1740-41 (2007) reaffirmed that "when the prior art ***teaches away*** from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious." *KSR*, 127 S. Ct. at 1740. That the cited art "teaches away" from the claimed invention is strong evidence showing nonobviousness of the claims. *Monarch Knitting Machinery Corp.*, 139 F.3d at 885.

Nor does the third reference Lowell fix the prior deficiencies. To simply overwrite a buffer perform what the claims require (1) tag, but not terminate, (2) set the tag bits indicative of overrun, (3) operate on the tag bits, not the data bits, and (4) use the "illegal" tag bits to result in aborting the frame.

Applicant's approach invents a tag not know in the prior art (hence the use of the mock "illegal") and operates in a new and non-obvious manner. None of the references alone or in combination fairly teach, or suggest, the Applicant's inventive approach. Allowance is earnestly solicited.

CONCLUSION

Applicant hereby request and petitions for a 3 month extension of time. The requisite fee is being paid electronically with this Amendment and Response. However, the

Commissioner is hereby authorized to charge any additional fees that may be required to Deposit Account No. 50-2862.

Favorable action on the merits of the claims is therefore earnestly solicited. If any issues remain, please contact Applicant's undersigned representative at (949) 760-9600.

Respectfully submitted,

O'MELVENY & MYERS LLP

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By: _____
David B. Murphy
Reg. No. 31,125

DBM/slc

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